## Claims

What is claimed is:

1. A method of reducing power consumption in a multi-way set-associative cache memory, comprising:

during a first clock cycle, in response to an address, identifying an associated set in the cache memory, comparing the address to respective tag portions of blocks in the associated set, and outputting a signal in response thereto; and

during a second clock cycle, in response to the signal indicating a match between one of the blocks and the address, reading a non-tag portion of the matching block in the associated set, while a non-matching block in the associated set is disabled.

2. The method of Claim 1, wherein the reading comprises:

enabling the non-tag portion of the matching block in the associated set.

3. The method of Claim 2, wherein the enabling comprises:

applying power to the non-tag portion of the matching block in the associated set.

4. The method of Claim 1, and comprising:

removing power from the non-matching block in the associated set.

5. The method of Claim 4, wherein removing power comprises:

removing power from the non-matching block in the associated set, so that the non-matching block in the associated set is disabled from outputting information, and so that the non-matching block in the associated set continues to store the information.

6. The method of Claim 1, wherein the cache memory is a program cache.

7. The method of Claim 1, wherein the cache memory is a data cache.

8. The method of Claim 1, wherein comparing the address comprises:

comparing a portion of the address to respective tag portions of blocks in the associated set.

9. The method of Claim 1, wherein reading the non-tag portion comprises:

reading the non-tag portion of the matching block in the associated set, while the non-matching block in the associated set is at least partly disabled.

10. The method of Claim 1, wherein reading the non-tag portion comprises:

reading the non-tag portion of the matching block in the associated set, while at least first and second non-matching blocks in the associated set are disabled.

11. A system for reducing power consumption in a multi-way set-associative cache memory, comprising:

first circuitry for: during a first clock cycle, in response to an address, identifying an associated set in the cache memory, comparing the address to respective tag portions of blocks in the associated set, and outputting a signal in response thereto; and

second circuitry for: during a second clock cycle, in response to the signal indicating a match between one of the blocks and the address, reading a non-tag portion of the matching block in the associated set, while a non-matching block in the associated set is disabled.

12. The system of Claim 11, wherein the second circuitry is for enabling the non-tag portion of the matching block in the associated set.

13. The system of Claim 12, wherein the second circuitry is for applying power to the non-tag portion of the matching block in the associated set.

14. The system of Claim 11, wherein the second circuitry is for removing power from the non-matching block in the associated set.

15. The system of Claim 14, wherein the second circuitry is for removing power from the non-matching block in the associated set, so that the non-matching block in the associated set is disabled from outputting information, and so that the non-matching block in the associated set continues to store the information.

16. The system of Claim 11, wherein the cache memory is a program cache.

17. The system of Claim 11, wherein the cache memory is a data cache.

18. The system of Claim 11, wherein the first circuitry is for comparing a portion of the address to respective tag portions of blocks in the associated set.

19. The system of Claim 11, wherein the second circuitry is for reading the non-tag portion of the matching block in the associated set, while the non-matching block in the associated set is at least partly disabled.

20. The system of Claim 11, wherein the second circuitry is for reading the non-tag portion of the matching block in the associated set, while at least first and second non-matching blocks in the associated set are disabled.